

# Contents

<b>List of Symbols .....</b>	xiii
<b>1 Silicon Properties .....</b>	1
1.1 Introduction .....	1
1.2 Valence-Bond and Two-Carrier Concept .....	1
1.2.1 Doping .....	3
1.3 Energy Bands in Silicon .....	6
1.3.1 Energy Band Model .....	6
1.3.2 Metals, Semiconductors and Insulators .....	10
1.3.3 Band Model for Impurities in Silicon .....	11
1.3.4 Energy Band Theory .....	12
1.3.5 Effective Mass .....	16
1.4 Thermal Equilibrium Statistics .....	17
1.4.1 The Boltzmann Distribution Function .....	18
1.4.2 Fermi-Dirac Distribution and Density of States .....	18
1.4.3 Density of States and Carrier Distribution in Silicon .....	20
1.4.4 Doped Silicon .....	23
1.5 Carrier Transport .....	28
1.5.1 Carrier Transport by Drift: Low Field .....	29
1.5.2 Matthiesson's Rule .....	36
1.5.3 Carrier Transport by Drift: High Field .....	37
1.5.4 Carrier Transport by Diffusion .....	42
1.6 Nonequilibrium Conditions .....	44
1.6.1 Carrier Lifetime .....	45
1.6.2 Diffusion Length .....	49
1.7 Problems .....	50
References .....	52
<b>2 Junctions and Contacts .....</b>	55
2.1 Introduction .....	55
2.2 PN Junction .....	55
2.2.1 Junction Profiles and Shapes .....	57

2.2.2	Step-Junction Approximation . . . . .	57
2.2.3	PN Junction at Thermal Equilibrium . . . . .	64
2.2.4	PN Junction in Forward Bias . . . . .	77
2.2.5	PN Junction in Reverse Bias . . . . .	93
2.3	Contacts . . . . .	111
2.3.1	Rectifying Contacts, Schottky Barrier Diode . . . . .	111
2.3.2	Current–Voltage Characteristics . . . . .	118
2.3.3	Ohmic Contacts . . . . .	123
2.4	Problems . . . . .	129
	References . . . . .	131
<b>3</b>	<b>The Bipolar Transistor . . . . .</b>	<b>135</b>
3.1	Introduction . . . . .	135
3.2	Transistor Action, a Qualitative Description . . . . .	136
3.2.1	Nomenclature and Regions of Operation . . . . .	136
3.2.2	Idealized Structure . . . . .	138
3.2.3	Ebers-Moll Equations . . . . .	141
3.2.4	Collector Saturation Voltage, $V_{CEsat}$ . . . . .	142
3.3	Planar Transistor, Low-Level Injection . . . . .	143
3.3.1	Low-Level Injection Parameters . . . . .	144
3.3.2	Collector-Base Reverse Characteristics . . . . .	151
3.3.3	Emitter-Base Reverse Characteristics . . . . .	156
3.3.4	Polysilicon Emitter and Interface Oxide . . . . .	158
3.3.5	Transistor Resistances . . . . .	165
3.4	High-Level Injection Effects . . . . .	172
3.4.1	Base Conductivity Modulation . . . . .	172
3.4.2	Base-Push Effect (Kirk Effect) . . . . .	173
3.5	Frequency Response of Current Gain . . . . .	175
3.5.1	Emitter Delay, $\tau_E$ . . . . .	176
3.5.2	Base Transit Time, $\tau_B$ . . . . .	177
3.5.3	Collector Delay, $\tau_C$ . . . . .	179
3.6	The Transistor as a Switch . . . . .	182
3.6.1	Delay Time, $t_d$ . . . . .	183
3.6.2	Rise Time, $t_r$ . . . . .	185
3.6.3	Storage Time, $t_s$ . . . . .	186
3.6.4	Fall Time, $t_f$ . . . . .	187
3.7	Silicon-Germanium Transistor . . . . .	188
3.7.1	SiGe Film Deposition and Properties . . . . .	188
3.7.2	Bandgap Lowering . . . . .	191
3.7.3	Density of States . . . . .	192
3.7.4	Mobility . . . . .	192
3.7.5	Transistor Parameters . . . . .	196
3.7.6	Transistor Optimization . . . . .	200
3.8	Problems . . . . .	204
	References . . . . .	207

<b>4 The MOS Structure . . . . .</b>	213
4.1 Introduction . . . . .	213
4.2 Physics of an Ideal <i>MOS</i> Structure . . . . .	214
4.2.1 Description of Semiconductor Surface Conditions . . . . .	215
4.2.2 Surface Charge and Electric Field . . . . .	220
4.2.3 Approximations . . . . .	222
4.2.4 Excess Surface Carrier Concentrations . . . . .	224
4.2.5 <i>MOS</i> Capacitance . . . . .	225
4.3 Calculation of Capacitance . . . . .	228
4.3.1 Calculation of Low-Frequency Capacitance . . . . .	228
4.3.2 Description of the Low-Frequency CV-Plot . . . . .	229
4.3.3 Calculation of High-Frequency Capacitance . . . . .	237
4.4 Measurement of <i>MOS</i> Capacitance . . . . .	239
4.4.1 Low-Frequency, or Quasi-Static CV Measurement . . . . .	239
4.4.2 High-Frequency CV Measurement . . . . .	240
4.5 Non-Uniform Impurity Profile . . . . .	241
4.5.1 Profile Approximations . . . . .	242
4.5.2 Surface Conditions . . . . .	242
4.6 Non-Ideal <i>MOS</i> Structure . . . . .	244
4.6.1 Workfunction Difference . . . . .	244
4.6.2 Dielectric Charge . . . . .	247
4.7 Characterization and Parameter Extraction . . . . .	253
4.7.1 Extraction of Equivalent Oxide Thickness, $t_{eq}$ . . . . .	253
4.7.2 Workfunction Difference . . . . .	254
4.7.3 Extraction of Dopant Concentration . . . . .	255
4.7.4 Lifetime Measurements . . . . .	257
4.7.5 Extraction of Interface-State Distribution . . . . .	259
4.7.6 Extraction of Mobile Ion Concentration . . . . .	263
4.8 Carrier Transport Through the Dielectric . . . . .	264
4.8.1 Tunneling Through the Oxide . . . . .	265
4.8.2 Avalanche Injection . . . . .	266
4.9 Problems . . . . .	268
References . . . . .	270
<b>5 Insulated-Gate Field-Effect Transistor . . . . .</b>	273
5.1 Introduction . . . . .	273
5.2 Qualitative Description of <i>MOSFET</i> Operation . . . . .	273
5.3 Gate-Controlled PN Junction, or Gated Diode . . . . .	277
5.3.1 Junction at Equilibrium . . . . .	277
5.3.2 Reverse Biased Junction: Depleting Gate Voltage . . . . .	279
5.3.3 Reverse Biased Junction: Accumulating Gate Voltage . . . . .	281
5.4 MOSFET Characteristics . . . . .	286
5.4.1 Long and Wide Channel . . . . .	286
5.4.2 Scaling to Small Dimensions . . . . .	304

5.4.3	Short-Channel Effects, <i>SCE</i> .....	312
5.4.4	Reverse Short-Channel Effects, <i>RSCE</i> .....	319
5.4.5	Narrow Channel Effects, <i>NCE</i> .....	322
5.4.6	Reverse Narrow-Channel Effects, <i>RNCE</i> .....	326
5.4.7	Small-Size Effects .....	329
5.5	Mobility Enhancement .....	330
5.5.1	Mean-Free Time Between Collisions, $\tau$ .....	331
5.5.2	Effective Mass .....	334
5.6	Ultrathin Oxide and High-K Dielectrics .....	340
5.6.1	High-K Dielectric Requirements .....	341
5.6.2	High-K Materials .....	343
5.7	Gate Stack .....	345
5.7.1	Polysilicon Workfunction .....	346
5.7.2	Metal Gates .....	347
5.8	Three-Dimensional Structures, <i>FinFETS</i> .....	352
5.9	Problems .....	353
	References .....	356
<b>6</b>	<b>Analog Devices and Passive Components</b> .....	369
6.1	Introduction .....	369
6.2	Analog Devices .....	370
6.2.1	Junction Field-Effect Transistor, JFET .....	370
6.2.2	Analog/RF MOSFETs .....	381
6.2.3	Integrated Passive Components .....	385
6.3	Matching .....	409
6.3.1	<i>MOSFET</i> Mismatch .....	410
6.3.2	Bipolar Transistor Mismatch .....	416
6.3.3	Resistor Mismatch .....	417
6.3.4	Capacitor Mismatch .....	419
6.4	Noise .....	422
6.4.1	Classification of Noise .....	423
6.5	Problems .....	429
	References .....	430
<b>7</b>	<b>Enabling Processes and Integration</b> .....	439
7.1	Introduction .....	439
7.2	A Conventional CMOS Logic Process Flow .....	439
7.3	A BiCMOS Process Flow .....	446
7.4	Advanced Enabling Processes .....	451
7.4.1	Crystal Growth and Wafer Preparation .....	451
7.4.2	Short-Duration Thermal Processes .....	460
7.4.3	Thin-Film Deposition .....	466
7.4.4	Integration of Ultra-Shallow Junctions .....	479
7.4.5	Gate Stack Module .....	485

Contents	xi
7.5 Advanced Interconnects .....	489
7.5.1 Copper Interconnects .....	491
7.5.2 Low-K Dielectrics .....	498
7.6 Problems .....	501
References .....	503
<b>8 Applications .....</b>	<b>523</b>
8.1 Introduction .....	523
8.2 Logic Units .....	523
8.2.1 The Inverter .....	523
8.2.2 The <i>CMOS</i> Inverter .....	528
8.2.3 The <i>BiCMOS</i> Inverter .....	533
8.2.4 <i>CMOS NAND</i> and <i>NOR</i> Gates .....	534
8.2.5 <i>BiCMOS</i> Two-Input <i>NAND</i> .....	535
8.2.6 The Transmission Gate .....	536
8.3 Memories .....	537
8.3.1 Dynamic Random-Access Memories, <i>DRAM</i> .....	537
8.3.2 Static Random Access Memories, <i>SRAM</i> .....	546
8.3.3 Nonvolatile Memory, <i>NVM</i> .....	551
8.3.4 <i>BiCMOS</i> for Analog/RF Applications .....	566
8.4 Problems .....	567
References .....	567
<b>Appendix A: Universal Physical Constants .....</b>	<b>575</b>
<b>Appendix B: International System of Units, SI .....</b>	<b>577</b>
<b>Appendix C: The Greek Alphabet .....</b>	<b>579</b>
<b>Appendix D: Properties of Silicon and Germanium (300 K, Intrinsic Semiconductor Unless Otherwise Stated) .....</b>	<b>581</b>
<b>Appendix E: Conversion Factors .....</b>	<b>583</b>
<b>Index .....</b>	<b>585</b>